**Amendments to the claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of claims:**

1. (Currently amended) A pipeline arrangement for memory access allocation of a network traffic scheduler comprising:

A hierarchical structure~~;~~ ~~A~~ comprising a physical port bandwidth that is divided into a plurality of logical links, the bandwidth available to each of the logical links is divided into a plurality of VLANs, and the bandwidth associated with each VLAN is shared by a plurality of individual user flows;

A plurality of SRAM and DRAM memory devices external to the scheduler, a first SRAM that contains a set of data buses and that stores flow queue control blocks that are required for 'read' and 'write' at each flow queue enqueue and dequeue time, and a second SRAM containing two data buses, one dedicated to 'read' and one dedicated to 'write', and that stores frame control blocks and VLAN hierarchy control blocks, a first DRAM that stores a network management counter and a second DRAM that stores flow queue control blocks and VLAN hierarchy control blocks that require 'read' only at both enqueue time and dequeue time;

Control blocks of scheduling elements stored in said memory devices with at least some of the memory devices storing more than one type of control block; wherein

a) SRAM memory is used if the content of a control block is Read-Modify-Write at packet enqueue and at dequeue;

b) SRAM and DRAM memory are used if the control block content is Read-Modify-Write only, at the packet dequeue;

c) DRAM memory is used if the control block content is Read only at packet enqueue and dequeue; and

d) Memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks;

Time based calendar arrays to provide guaranteed bandwidth service for flow queues and VLANs; and

Weighted fair queueing calendar arrays for allocation of available bandwith for competing flows when no service is required by time base calendars.

2. (Previously Presented) The arrangement according to claim 1 wherein DRAM memory is preferentially used if the Read-Modify-Write content is only at a packet dequeue.

3-4. (Canceled)

5. (Currently Amended) The pipeline arrangement for memory access allocation according to claim 1 wherein the pipeline arrangement also includes non-hierarchical link sharing whereby physical port bandwidth resources are shared among individual traffic flows.

6-24. (Canceled)